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10EC751

Seventh Semester B.E. Degree Examination, Dec.2015/Jan.2016
DSP Algorithm and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What is digital signal processing? List the unique architectural features of DSP processor. **(05 Marks)**

b. "FIR filter are linear phase filters". Justify the same with magnitude and phase plots. **(05 Marks)**

c. With the help of block diagram and equations explain decimation and interpolation process. Also find interpolated O/P sequence for x(n) = {0, 3, 6, 9} with b_k = {⅓, ⅔, 1, ⅔,⅓ } and interpolation factor in 2. **(10 Marks)**

2 a. Give the structure of 4 × 4 drawn multiplier explain its concept. What modification in required to carryout multiplication of signed no's? Comment on the speed of the multiplier. **(08 Marks)**

b. Explain the circular and bit reversed addressing mode, with the help of algorithm. **(08 Marks)**

c. What are the memory address of the operands in each of the following cases of indirect addressing model? In each case what will be the content of address register after the memory access? Assume that the initial contents of address register and the offset register are 0300h and 0020h.
i) ADD *addreg$^-$ ii) ADD $^+$*addreg iii) ADD $^+$*offset, *addreg iv) ADD *addreg, offset$^-$. **(04 Marks)**

3 a. Compare architectural features of TMS320C25 and ADSP2100 fixed point DSPs. **(05 Marks)**

b. Explain the PMST register. Also explain the direct addressing mode of TMS320C54XX processor, with the help of a block diagram. **(09 Marks)**

c. Explain the CPU unit of TMS320C54XX processor with the help of functional diagram. **(06 Marks)**

4 a. Describe the operation of the following instructions of TMS320C54XX processor with example :
i) MAC ii) RPT iii) MPY. **(06 Marks)**

b. Describe the operation of hardware timer with a neat diagram. **(08 Marks)**

c. Write an assembly language program of TMS320C54XX processor to compute the sum of three product terms given by the equation :
$y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$,
using MAC instruction. **(06 Marks)**

PART – B

5 a. Determine the value of each of the following 16 bit numbers represented using the given Q-notation.
i) 4400h or Q_0 ii) 4400h or Q_{15} iii) 4400h or Q_7 iv) 4400h or Q_1. **(06 Marks)**

b. What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase subfilter. Write the program. **(08 Marks)**

c. Write a program to multiply two Q_{15} numbers. **(06 Marks)**

6 a. i) Derive the equation to implement a Butterfly structure in DITFFT algorithm
ii) How many add/substract and multiply operations are needed to compute the butterfly structure?
iii) Determine the optimum scaling factor. **(08 Marks)**

b. i) What minimum size FFT must be used to compute a DFT of 40 sample?
ii) How many stages are required for FFT computation?
iii) How many butterflies there per stage?
iv) How many butterflies are needed for the entire computation? **(06 Marks)**

c. Write the subroutine for bit reverse address generation. Explain the same. **(06 Marks)**

7 a. Explain briefly memory space organisation in TMS320C54XX memory. **(04 Marks)**

b. Describe DMA with respect to TMS320C54XX processor. **(08 Marks)**

c. What are Interrupts? How interrupts are handled by the C54XX DPS processors. **(08 Marks)**

8 a. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals. **(06 Marks)**

b. Write a pseudo algorithm for determining heart rate (HR) using the digital signal processor. **(06 Marks)**

c. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(08 Marks)**

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